Mayukh Sarkar

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Current Engagement

Currently engaged as *Assistant Professor* in the *Department of Computer Science and Engineering* at *Motilal Nehru National Institute of Technology Allahabad* since *01.07.2019*

Previous Engagements

Teaching Experience

14.06.2018–25.07.2018 **Assistant Professor, Department of Computer Science and Engineering**, *Techno India University West Bengal*, Kolkata.

27.07.2018–12.07.2019 **Assistant Professor (Temporary), Department of Computer Science and Engineering**, *National Institute of Technology Sikkim*.

Industrial Experience

26.07.2010–08.07.2011 **Programmer Analyst Trainee**, *Cognizant Technology Solutions*, Kolkata.

Academic Background

2013–13.06.2018 **Ph.D. Scholar**, *Indian Institute of Engineering Science and Technology*, Shibpur, Thesis Topic – Design, Optimization and Realization of Computing Algorithms on a DNA Computer.

2011–2013 **M.E. in Information Technology**, *Bengal Engineering and Science University*, Shibpur, *Marks – 75.61%*.
Thesis Topic – Study and Design of Algorithms for Synthesis of Reversible Logic Circuits

2006–2010 **B.Tech. in Computer Science and Engineering**, *Govt. College of Engineering and Ceramic Technology*, University – West Bengal University of Technology.
Grade – 7.99 DGPA

2005 **Higher Secondary(10+2) in Science**, *B.E. College Model School*, Board – West Bengal Council of Higher Secondary Education, *Marks – 72.3%*.

2003 **Secondary(10)**, *B.E. College Model School*, Board – West Bengal Board of Secondary Education, *Marks – 83.37%*.

Doctorate thesis

title *Design, Optimization and Realization of Computing Algorithms on a DNA Computer*

supervisor Dr. Prasun Ghosal, *Asst. Professor, Dept. of IT, IIEST, Shibpur*

description With the tremendous growth in VLSI technology following the Moore's law, the integration density of transistors has reached billions. This has caused scaling of transistors to reach subatomic dimension in DSM (deep submicron regime), resulting in failure of classical physics. Hence, the classical computing technology has reached a physical limit, and slowing down of Moore's law. Also, at such small size, current leakage becomes a problem in classical technology, which heats up the chip, and hence Dennard scaling, which states about the constant power density with the decrease of transistor size, also fails. It causes the switch to multi-core technology, but it also seems to be at the end due to Dark Silicon problem. So, one promising solution of these problems is to switch to some non-CMOS technology, such as, Quantum Computing, bio-inspired computing such as DNA, etc. Not only due to the problems currently being faced in conventional technology, the main reasons behind the fame of DNA computing are manifold, such as, massively parallel operations, huge information density over silicon etc.. Due to these massive advantages, DNA computing has been proved to be fruitful for solving computationally "hard" problems in polynomial operations, such as, Hamiltonian Circuit Path problem, 3-SAT problem etc. Even with these tremendous powers, the DNA computing still lacks the ability to perform general applications applicable on a conventional computer due to its lack of proper ALU or data structure as available for conventional computer. This work targets to fill up the gap by designing an automated ALU and data structures and designing a complete hypothetical DNA machine, so that, the DNA computer also become capable in performing the conventional applications and thus can be a fruitful replacement of the conventional silicon-based computing.

M.E. Thesis

Title *Study and Design of Algorithms for Synthesis of Reversible Logic Circuits*

Supervisor Dr. Prasun Ghosal, *Asst. Professor, Dept. of IT, IIEST, Shibpur*

Description Due to inherent information loss and other factors associated with irreversible computing, reversible circuits are becoming more and more important. Synthesis of reversible circuits, defined as the ability to generate an efficient circuit from a given arbitrary-size specification. Working on synthesis methods for reversible circuits has received a significant attention recently. In this thesis, two algorithms have been proposed for the synthesis. Both of these algorithms are using traditional Quine-McCluskey method in modified manner. The first algorithm is performing functional synthesis. The second algorithm is a stochastic procedure, performing direct synthesis of the reversible circuit.

B.Tech. Project

Final Year Project

Title *C Compiler Design using C*

Supervisor Mr. Partha Ghosh, *Department of Computer Science and Engineering, Govt. College of Engineering and Ceramic Technology, Kolkata*

Summer Training

Title *Library Management System Using .NET*

Organization CMC Ltd.

Research Interests

1. DNA Computing
2. Design and Analysis of Algorithms
3. Quantum and Reversible Computing

Subjects of Interests

1. Data Structures, and Design and Analysis of Algorithms
2. Operating Systems
3. Compiler Design

Languages

Bengali Reading, Writing, Speaking
English Reading, Writing, Speaking
Hindi Reading, Writing, Speaking

Publications

Book Chapter

1. P. Ghosal, **M. Sarkar**, and P. Chatterjee, "A New Paradigm towards Performance Centric Computation beyond CMOS: DNA Computing", in *Nano-CMOS and Post-CMOS Electronics: Vol 2. Circuits and Design, The Institute of Engineering and Technology (IET)*, Chapter 12, pp. 379-408, DOI: 10.1049/PBCS030E_ch12.

Journal

1. **M. Sarkar**, P. Ghosal, and S.P. Mohanty, "Minimal Reversible Circuit Synthesis on a DNA Computer". in *Natural Computing, Springer*, Volume 16, Issue 3, pp. 463-472, September 2017.
2. **M. Sarkar**, P. Ghosal, and S.P. Mohanty, "Exploring the Feasibility of a DNA Computer: Design of an ALU Using Sticker-Based DNA Model". in *IEEE Transactions on NanoBioscience*, Volume 16, No. 6, pp. 383-399, Sept. 2017.

Conference Paper

1. **M. Sarkar**, P. Ghosal, and S.P. Mohanty, "Reversible Circuit Synthesis using ACO and SA based Quine-McCluskey method" in *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Columbus, OH, 2013, pp. 416-419.
2. **M. Sarkar** and P. Ghosal, "Implementing Data Structure Using DNA: An Alternative in Post CMOS Computing" in *2015 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Montpellier, 2015, pp. 345-349.
3. P. Chatterjee, **M. Sarkar** and P. Ghosal, "Computing in Ribosomes: Performing Boolean Logic Using mRNA-Ribosome System" in *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Pittsburgh, PA, 2016, pp. 260-265.

4. **M. Sarkar** and P. Ghosal, "Mathematics using DNA: Performing GCD and LCM on a DNA Computer". in *2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, Gwalior, 2016, pp. 240-243.
5. P. Chatterjee, **M. Sarkar** and P. Ghosal, "Computing in Ribosomes: Implementing Sequential Circuits using mRNA-Ribosome System". in *2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, Gwalior, 2016, pp. 230-235.
6. **M. Sarkar**, and P. Ghosal, "Post CMOS Computing Beyond Si: DNA Computer as Future Alternative" in *2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, Gwalior, 2016, pp. 129-133.
7. S. Shakhari, P. Ghosal, and **M. Sarkar**, "A Provably Good Method to Generate Good DNA Sequences" in *2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, Gwalior, 2016, pp. 134-138.
8. **M. Sarkar**, and P. Ghosal, "Performing Mathematics Using DNA: Complex Number Arithmetic Using Sticker Model" in *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Bochum, 2017, pp. 568-573.

Technical Reports

1. P. Ghosal, and **M. Sarkar**, "Beyond Silicon: Is DNA Computer Going to be the Future?" in *VLSI Circuits and Systems Letter*, Volume 1, Issue 1, April 2015.
2. P. Ghosal, P. Chatterjee, and **M. Sarkar**, "Bringing out a Natural Computer (Ribosome) from within a Cell: A Next-Gen Alternative?" in *VLSI Circuits and Systems Letter*, Volume 2, Issue 1, April 2016.

Awards and Recognitions

1. Awardee of **TCVLSI (Technical Committee on VLSI) Student Travel Grant Award** for 2015 IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2015) to present the paper "Implementing Data Structure Using DNA: An Alternative in Post CMOS Computing".
2. **Best Paper Award** at 2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS 2016) for the paper "Computing in Ribosomes: Implementing Sequential Circuits using mRNA-Ribosome System".

Additional Informations

1. Selected as team member for participating in "4th Quazi Azher Ali International Programming Contest 2014" organized at Bangladesh University.
2. Participated in State Telegraph Junior Chess Tournament at the age of 6.
3. Participated in National Chess Tournament, 2010.
4. Participated in District Badminton Tournament in 2002.

Personal Profile

Date of Birth Wednesday 23rd September, 1987

Father's Name	Mr. Manindra Nath Sarkar
Mother's Name	Mrs. Mira Sarkar
Nationality	Indian
Gender	Male
Marital Status	Single
Hobbies	Competitive Programming, Software Development, Experimenting with Linux, Reading Books, Playing Chess